SEMICONDUCTOR MEMORY DEVICE HAVING PARTIALLY CONTROLLED DELAY LOCKED LOOP

Abstract of the Disclosure

A semiconductor memory device having a partially controlled delay locked loop includes a delay locked loop and a control signal generator. The control signal generator generates a first control signal and a second control signal, which are responsive to first through fifth mode selection signals for selecting operation modes of the semiconductor memory, device to partially turn the delay locked loop on or off. If the first control signal or the second control signal is activated, a portion of the delay locked loop to which the first or second control signal is applied is turned off. If the first control signal or the second control signal is deactivated, a portion of the delay locked loop to which the first or second control signal is applied is turned on. If the first mode selection signal is activated, only the second control signal is activated. If the second mode selection signal is activated, the first and second control signals are deactivated. If at least one of the third through fifth mode selection signals is activated, the first and second control signals are activated. Since the semiconductor memory device includes a built-in delay locked loop which is partially turned on or off, current consumption of the semiconductor memory device can be reduced.

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